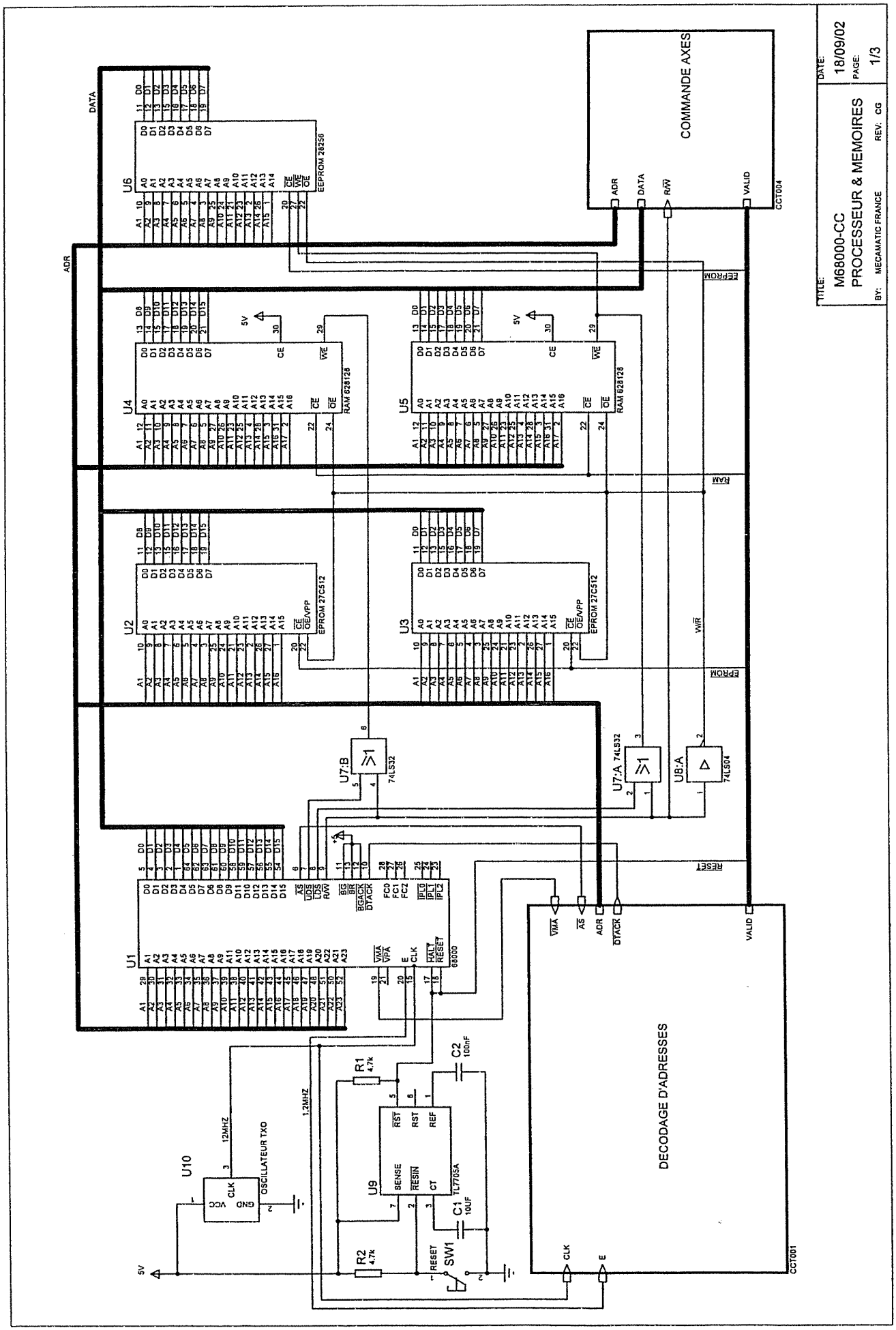
CENTRE D'USINAGE

DOSSIER DES SCHEMAS CONSTRUCTEUR

Ce dossier comporte les schémas des parties traitées dans ce sujet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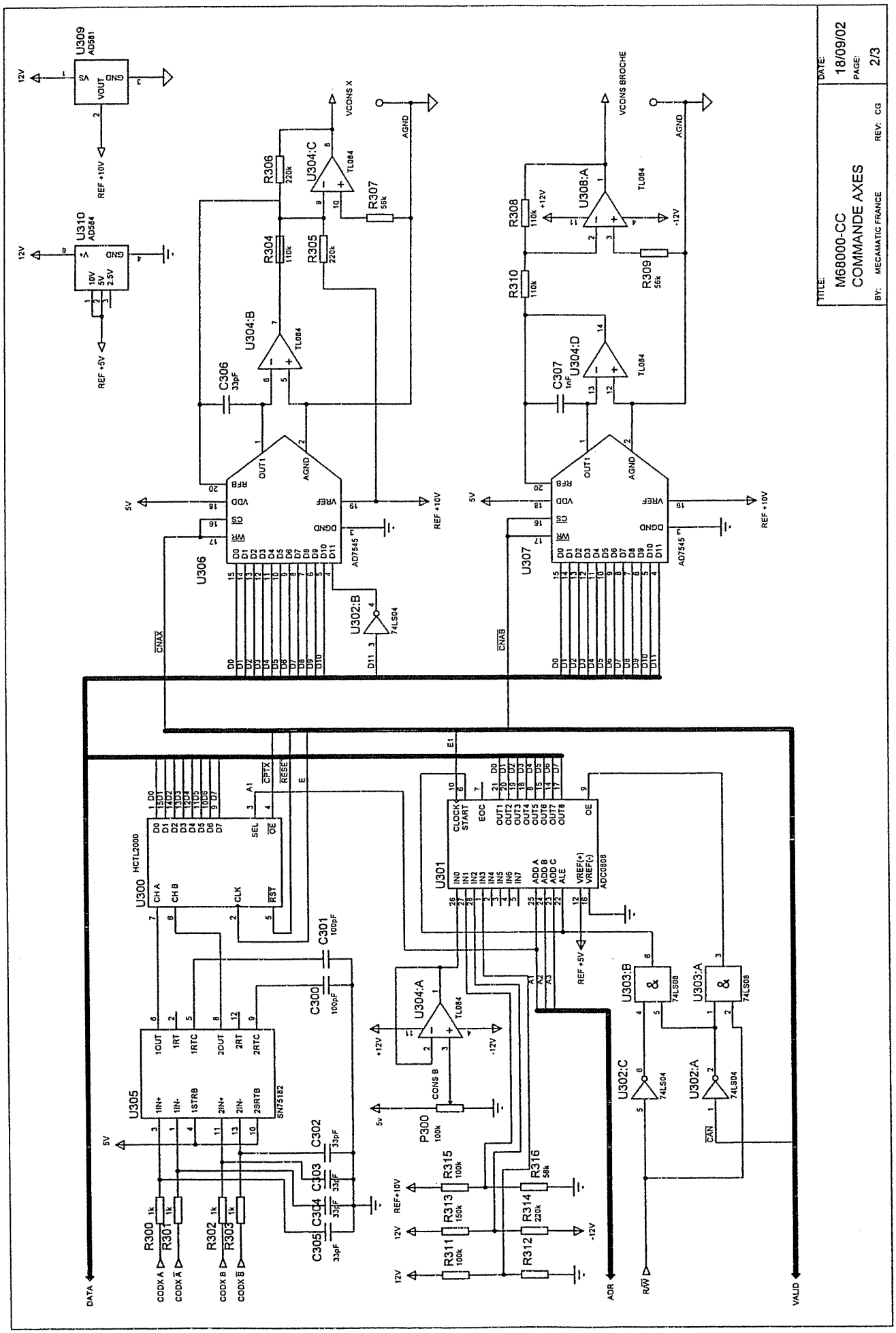
PROCESSEUR & MEMOIRES
BY: MECAMATIC FRANCE
REV: CG
DATE:
18/09/02
PAGE:
1/3
COMMANDE AXES
ADR
DATA
R/W
VALID
CCT004
DATA
ADR
EEPROM
RAM
EPROM
WR
RESET
U1
68000
U2
EPROM 27C512
U3
EPROM 27C512
U4
RAM 628128
U5
RAM 628128
U6
EEPROM 28256
U7:A 74LS32
U7:B 74LS32
U8:A 74LS04
U9
TL7705A
U10
OSCILLATEUR TXO
12MHZ
1.2MHZ
R1 4.7k
R2 4.7k
C1 10UF
C2 100nF
SW1
RESET
5V
VMA
AS
ADR
DTACK
VALID
CLK
E
DECODAGE D'ADRESSES
CCT001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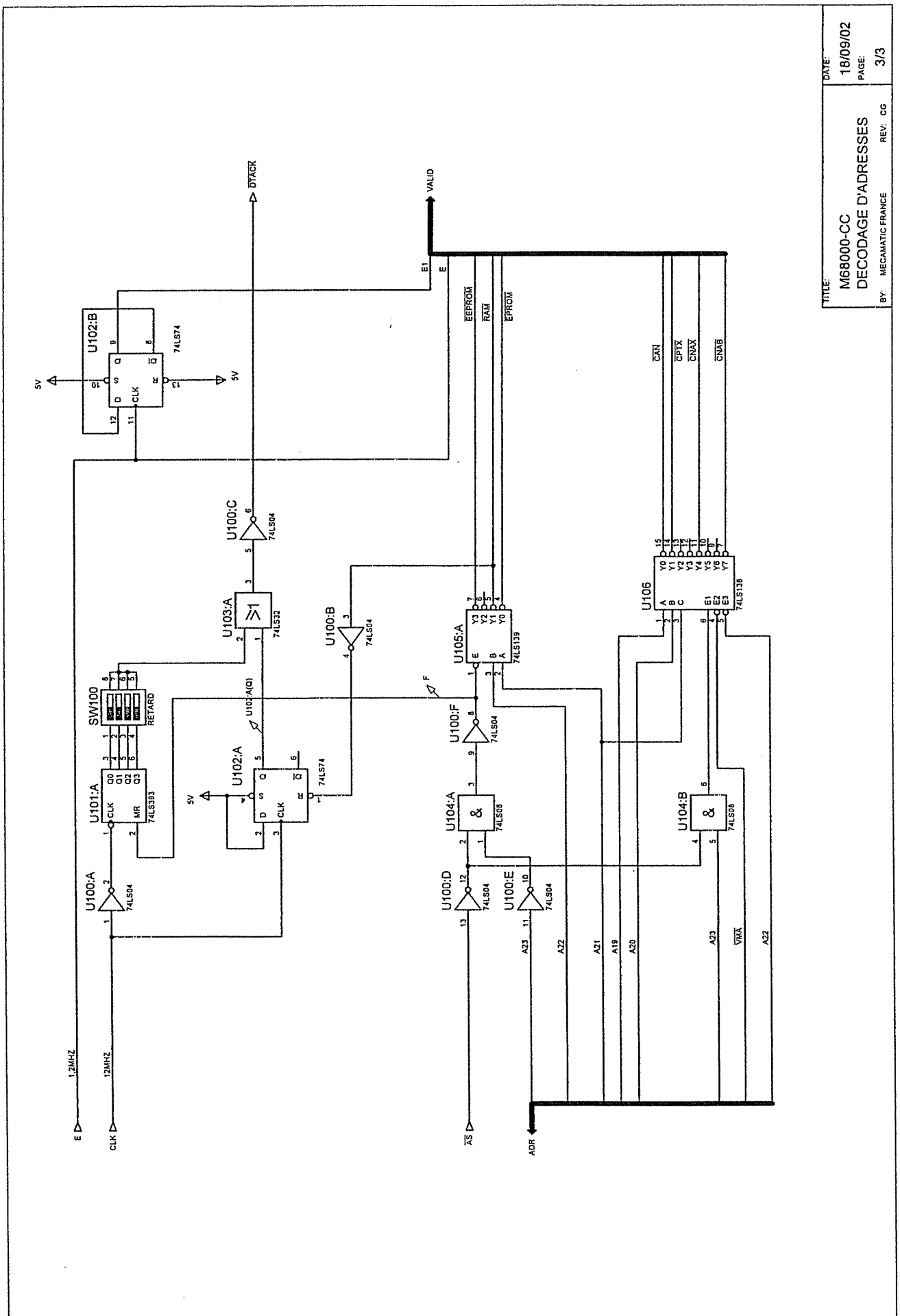
DATE: 18/09/02
PAGE: 2/3
U309 AD581
U310 AD584
REF +10V
REF +5V
U304:C TL084
U304:B TL084
U304:D TL084
U304:A TL084
U308:A TL084
VCONS X
VCONS BROCHE
AGND
R306 220k
R307 56k
R304 110k
R305 220k
R308 110k
R309 56k
R310 110k
C306 33pF
C307 1nF
U306 AD7545
U307 AD7545
U302:B 74LS04
U300 HCTL2000
U301 ADC0808
U305 SN75182
C301 100pF
C300 100pF
C302 33pF
C303 33pF
C304 33pF
C305 33pF
P300 100k
R315 100k
R316 56k
R313 150k
R314 220k
R311 100k
R312 100k
U303:B 74LS08
U303:A 74LS08
U302:C 74LS04
U302:A 74LS04
R300 1k
R301 1k
R302 1k
R303 1k
CODX A
CODX Ā
CODX B
CODX B̄
DATA
ADR
R/W̄
VALID
CNAX
CNAB
CAN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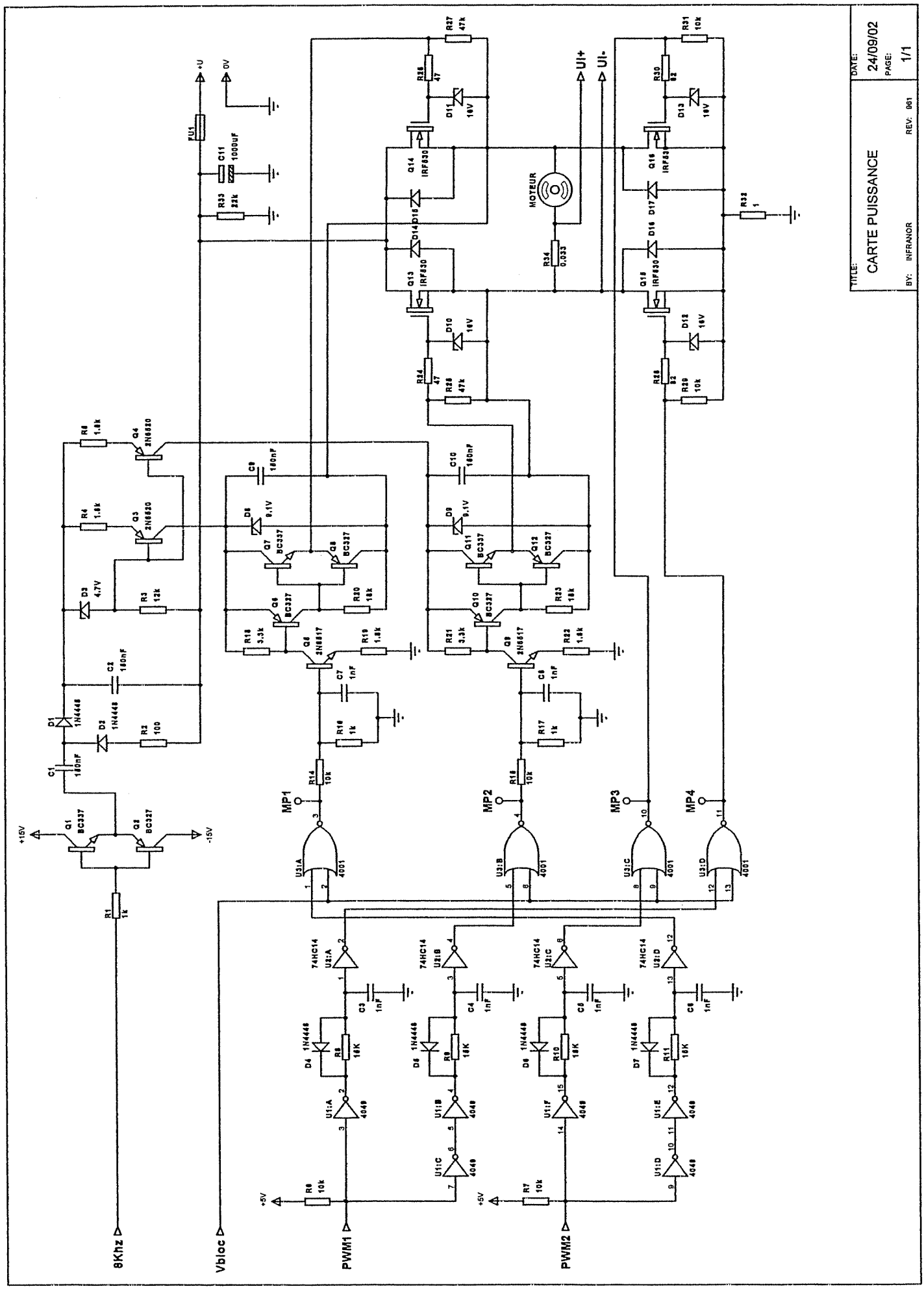
REV: CG
DATE:
18/09/02
PAGE:
3/3
DTACK
VALID
U102:B
74LS74
U100:C
74LS04
U103:A
74LS32
U100:B
74LS04
U105:A
74LS139
U106
74LS138
SW100
RETARD
U101:A
74LS393
U102:A
74LS74
U100:F
74LS04
U104:A
74LS08
U104:B
74LS08
U100:A
74LS04
U100:D
74LS04
U100:E
74LS04
EEPROM
RAM
EPROM
CAN
CPTX
CNAX
CNAB
1.2MHZ
12MHZ
E
CLK
AS
ADR
A23
A22
A21
A19
A20
VMA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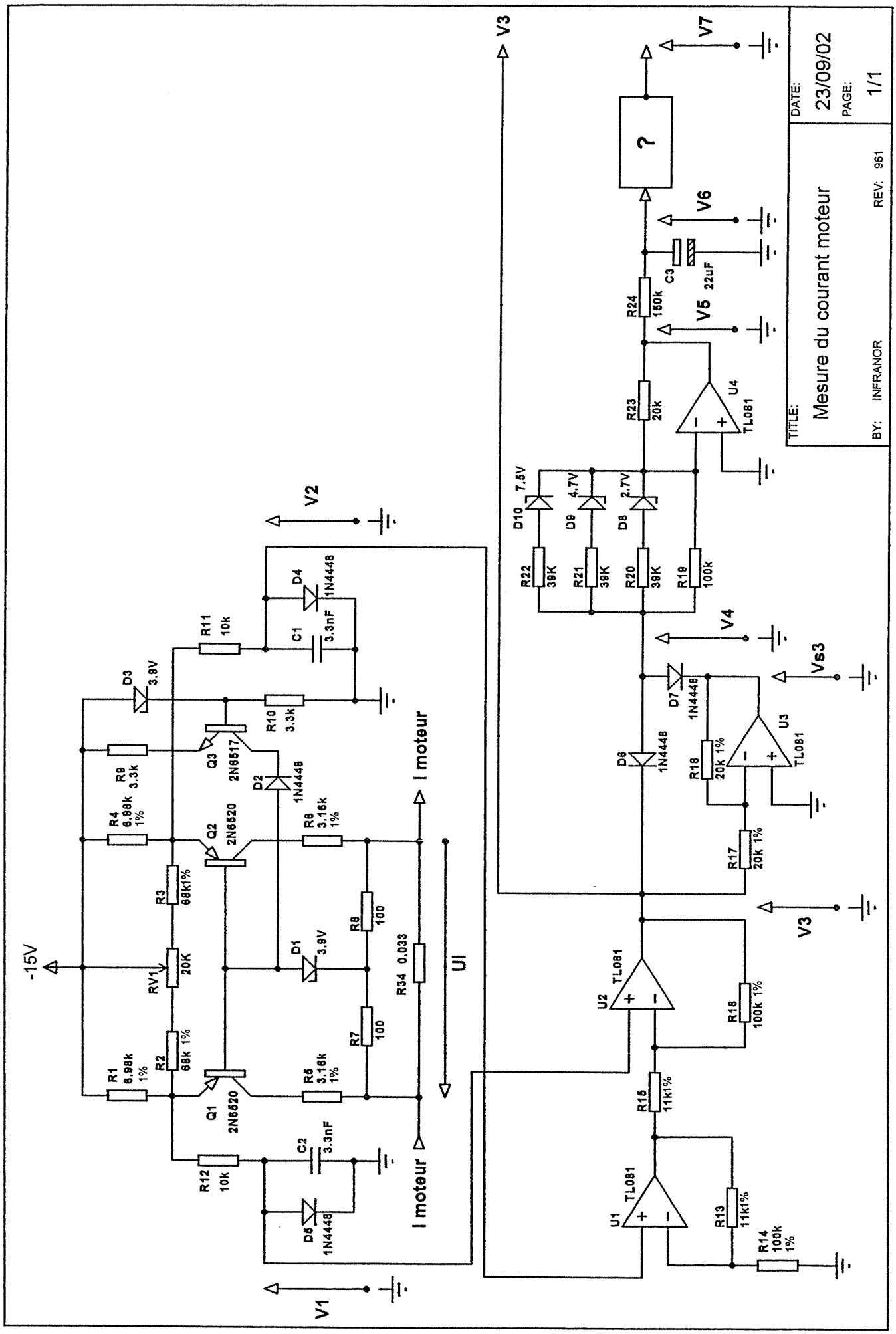
BY: INFRANOR
REV: 001
MOTEUR
UI+
UI-
+U
0V
8Khz
Vbloc
PWM1
PWM2
MP1
MP2
MP3
MP4
+15V
-15V
+5V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BY: INFRANOR
REV: 961
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-15V
V1
V2
V3
V4
V5 22uF
V6
V7
Vs3
I moteur
UI
?
R1 6.98k 1%
R2 68k 1%
R3 68k1%
R4 6.98k 1%
R5 3.16k 1%
R6 3.16k 1%
R7 100
R8 100
R9 3.3k
R10 3.3k
R11 10k
R12 10k
R13 11k1%
R14 100k 1%
R15 11k1%
R16 100k 1%
R17 20k 1%
R18 20k 1%
R19 100K
R20 39K
R21 39K
R22 39K
R23 20k
R24 150k
RV1 20K
C1 3.3nF
C2 3.3nF
C3
D1 3.8V
D2 1N4448
D3 3.8V
D4 1N4448
D5 1N4448
D6 1N4448
D7 1N4448
D8 2.7V
D9 4.7V
D10 7.5V
R34 0.033
Q1 2N6520
Q2 2N6520
Q3 2N6517
U1 TL081
U2 TL081
U3 TL081
U4 TL081

CENTRE D'USINAGE

DOCUMENTATION TECHNIQUE

Ce dossier comporte les documents techniques partiels des composants suivants :

Standard specifications

	Item	Type No.	Symbol	Unit(SI)	V4 V402-011	V4 V404-012	V4 V406-012	V5 V506-012	V5 V511-012
Motor	Rated output		P_R	W	23	40	60	60	110
	Rated armature voltage		V_R	V	20	72	70	75	75
	Rated torque		T_R	N·m	0.074	0.13	0.19	0.19	0.34
	Rated armature current		I_R	A	1.8	1.0	1.4	1.2	2.0
	Rated speed		N_R	min^{-1}	3000	3000	3000	3000	3000
	Continuous torque at stall		T_S	N·m	0.08	0.14	0.20	0.24	0.42
	Peak torque		$T_P(N)$	N·m	0.42	0.76	1.2	1.8	3.4
	Armature current at stall		I_S	A	1.8	0.9	1.4	1.3	2.1
	Peak armature current		$I_P(N)$	A	10	4.7	7.6	10	18
	Maximum speed		N_{max}	min^{-1}	5000	5000	5000	5000	5000
	Static friction torque		T_f	N·m	0.015	0.019	0.020	0.02	0.022
	Rated power rate		Q_R	kW/s	1.2	2.1	3.2	1.6	3.2
	Peak angular acceleration		α_P	rad/s^2	90×10^3	92×10^3	115×10^3	80×10^3	94×10^3
	Torque ripple		K_{Tr}	%	12	12	12	5.5	5.5
	Viscous damping constant		F_d	$N\cdot m/min^{-1}$	0.003×10^{-3}	0.006×10^{-3}	0.008×10^{-3}	0.009×10^{-3}	0.013×10^{-3}
	Torque constant		K_T	N·m/A	0.047	0.174	0.177	0.183	0.21
	Voltage constant		K_E	V/min^{-1}	4.9×10^{-3}	18.2×10^{-3}	18.5×10^{-3}	19.1×10^{-3}	21.8×10^{-3}
	Rotor moment of inertia		J_M	$kg\cdot m^2$	0.0047×10^{-3}	0.0084×10^{-3}	0.0108×10^{-3}	0.022×10^{-3}	0.037×10^{-3}
	Armature resistance		R_a	Ω	2.8	16.2	10.0	11.7	4.8
	Armature inductance		L_a	mH	0.9	4.2	3.4	5.0	2.4
	Mechanical time constant		t_m	ms	6.0	4.5	3.4	7.4	4.1
	Electrical time constant		t_e	ms	0.32	0.26	0.34	0.45	0.50
	Thermal time constant		$t\theta$	min	15	20	25	20	30
	Thermal resistance		$R\theta$	K/W	4.9	3.6	3.0	2.8	2.4
	Maximum temperature rise		θ	K	105	105	105	105	105
	Weight		W_M	kg	0.25	0.4	0.5	0.65	0.95
Tachometer generator	Voltage gradient		K_{EG}	V/min^{-1}	$3\times10^{-3}\pm10\%$			$7\times10^{-3}\pm10\%$	
	Ripple (rms)		ε_S	%	2			1	
	Ripple (p-p)		ε_R	%	5			3	
	Linearity		δ_L	%	1			1	
	Armature resistance		R_I	Ω	37			26	
	Armature inductance		L_I	mH	5			4.1	
	Minimum load resistance		R_L	kΩ	10			10	
	Rotor moment of inertia		J_{TG}	$kg\cdot m^2$	0.0011×10^{-3}			0.012×10^{-3}	
	Weight		W_T	kg	0.09			0.26	
Brake	Holding torque		T_B	N·m				0.29	
	Voltage		V_B	V.DC				90	
	Current		I_B	A				0.06	
	Winding resistance		R_B	Ω				1600	
	Moment of inertia		J_B	$kg\cdot m^2$				0.001×10^{-3}	
	Weight		W_B	kg				0.26	
Optical encoder		Open collector			200 500 1000 P/R				
		Line driver			200 500 1000 P/R				
Gear					1/12.5 1/25 1/50			1/15 1/30 1/60 1/90	
Oil seal								Oil seal Mountable	
Applicable servo amplifier standard type No.					DA2E020	DA2D020			

Gear ratings

Type No.	Code on motor type	Gear type No.		GA	GB	GC		G1	G2	G3	G4		G6	G7	G8	G9
				G6-12	G6-25	G6-50		G8-15	G8-30	G8-60	G8-90		G10-15	G10-30	G10-60	G10-90
Reduction ratio (nominal)			G6 gear	1/12.5	1/25	1/50	G8 gear	1/15	1/30	1/60	1/90	G10 gear	1/15	1/30	1/60	1/90
Reduction ratio (detailed)				1/12.5	1/25	1/50		1/15.004	1/31.155	1/60.227	1/89.588		1/15.303	1/30.066	1/60.132	1/90.198
Rated torque	T_{RG}	N·m		0.5	1.0	2.0		1.0	2.0	4.0	4.0		3.8	7.5	15.0	15.0
Peak torque	T_{PG}	N·m		1.5	3.0	6.0		3.0	6.0	12.0	12.0		12.0	23.0	45.0	45.0
Weight	W_G	kg		0.4				0.6					1.5			
Applicable motor				V4				V5					V7			

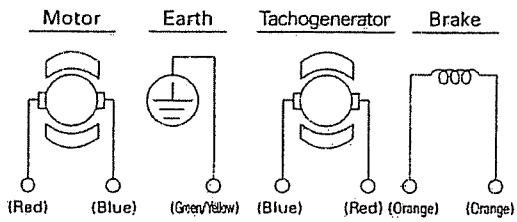
1. Do not use the unit beyond either rated or peak torque
2. If the unit is used beyond peak torque, the encoder may malfunction due to the thrust load

V7		V8		Term
V720 012	V730 012	V840 012	V850 012	
200	300	400	500	☆☆
80	75	85	80	☆☆
0.64	1.18	1.57	1.96	☆☆
3.3	5.2	5.8	7.6	☆☆
3000	2500	2500	2500	☆☆
0.77	1.43	1.70	2.16	☆☆
5.4	9.8	12.0	16.7	☆☆
3.7	5.5	6.0	7.6	☆☆
25	40	40	62	☆☆
5000	4000	4000	3000	
0.04	0.05	0.06	0.07	☆
2.7	5.1	5.0	6.4	☆☆
36×10^{3}	36×10^{3}	24×10^{3}	28×10^{3}	☆☆
3.5	3.5	2.5	2.5	☆
0.020×10^{-3}	0.039×10^{-3}	0.045×10^{-3}	0.058×10^{-3}	☆
0.23	0.273	0.302	0.287	☆
24.2×10^{-3}	28.6×10^{-3}	31.6×10^{-3}	30.0×10^{-3}	☆
0.147×10^{-3}	0.270×10^{-3}	0.50×10^{-3}	0.60×10^{-3}	
2.8	1.1	0.95	0.56	☆
3.0	1.6	1.9	1.1	☆
7.8	4.0	5.2	4.1	☆
1.1	1.5	2.0	1.9	☆
30	30	30	40	☆☆
1.2	1.2	1.1	1.0	☆☆
105	105	105	105	☆☆
1.8	2.5	3.4	4.0	
$7\times10^{-3}\pm10\%$				☆
1				☆
3				☆
1				☆
26				☆
4.1				☆
10				☆
0.012×10^{-3}				
0.35		0.45		
1.47		1.96		☆☆
90		90		☆
0.11		0.11		☆
820		820		☆
0.009×10^{-3}		0.02×10^{-3}		
0.59		0.79		
200 500 1000 P/R				
200 500 1000 2000 2500 P/R				
1/15 1/30 1/60 1/90				
Oil seal Mountable				
DA2D020		DA2D030		

Common specifications

Rating	Continuous (S1)
Insulation class	F
Excitation system	Permanent magnet
Insulation resistance	10MΩ or more (DC500V megger)
Dielectric strength	AC50Hz 1500V (600V for 24V spec. and TG); 1 minutes. (Do not test the insulation between the machine and the encoder.)
Rotation	Bi-directional
Ambient temperature	0 to 40°C
Humidity	20 to 90%RH (without dew)
Paint color	Black
Protection	Totally enclosed (IP43)

Connecting



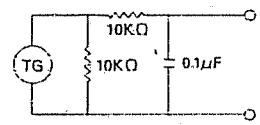
Motor rotation direction

When (Red) is positive (+) and (Blue) is negative (−), the motor rotates counterclockwise when viewed from the output shaft side.

Tachometer generator polarity

When the tachometer generator rotates counterclockwise when viewed from the output shaft side, (Red) becomes positive (+) and (Blue) becomes negative (−).

1) The items marked ☆ are specifications under 25°C ambient and armature coil temperature conditions.
The items marked ☆☆ are specifications during temperature rise saturation.
2) The values in the left table are obtained when a smooth direct current is used under 40°C or lower ambient temperature.
3) The tachometer generator characteristics were obtained using the test circuit below.



4) The values in the left table were measured by placing the machine on an aluminum plate.
V4 type=(150×150×t6), V5 type=(200×200×t12), V7 and V8 types=(305×305×t12)
5) An encoder cannot be mounted to a V4 type machine with a tachometer generator.
6) Do not use a holding brake as an emergency stopper.
7) In case of V404 and V406, specification is at rated armature voltage of 24V.
8) 24VDC operating brake is optionally available.

※For servo amplifier's details, refer to another "DA2" DC servo amplifier catalog.

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS74A
Dual Positive-Edge-Triggered D Flip-Flops with Preset, Clear and Complementary Outputs

General Description

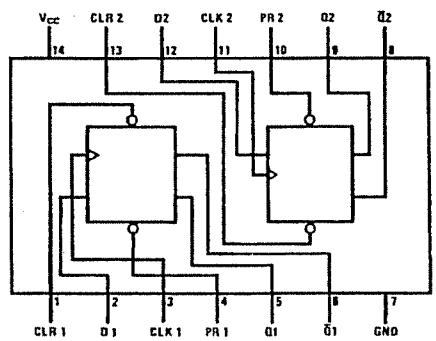
This device contains two independent positive-edge-triggered D flip-flops with complementary outputs. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. The triggering occurs at a voltage level and is not directly related to the transition time of the rising edge of the clock. The data on the D input may be changed while the clock is LOW or HIGH without affecting the outputs as long as the data setup and hold times are not violated. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs.

Ordering Code:

Order Number	Package Number	Package Description
DM74LS74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150 Narrow
DM74LS85ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Function Table

Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

 DS006373

FAIRCHILD
SEMICONDUCTOR™

August 1986
Revised March 2000

DM74LS138 • DM74LS139
Decoder/Demultiplexer

General Description

These Schottky-clamped circuits are designed to be used in high-performance memory-decoding or data-routing applications, requiring very short propagation delay times. In high-performance memory systems these decoders can be used to minimize the effects of system decoding. When used with high-speed memories, the delay times of these decoders are usually less than the typical access time of the memory. This means that the effective system delay introduced by the decoder is negligible.

The DM74LS138 decodes one-of-eight lines, based upon the conditions at the three binary select inputs and the three enable inputs. Two active-low and one active-high enable inputs reduce the need for external gates or inverters when expanding. A 24-line decoder can be implemented with no external inverters, and a 32-line decoder requires only one inverter. An enable input can be used as a data input for demultiplexing applications.

The DM74LS139 comprises two separate two-line-to-four-line decoders in a single package. The active-low enable input can be used as a data line in demultiplexing applications.

All of these decoders/demultiplexers feature fully buffered inputs, presenting only one normalized load to its driving circuit. All inputs are clamped with high-performance Schottky diodes to suppress line-ringing and simplify system design.

Features

- Designed specifically for high speed:
  - Memory decoders
  - Data transmission systems
- DM74LS138 3-to-8-line decoders incorporates 3 enable inputs to simplify cascading and/or data reception
- DM74LS139 contains two fully independent 2-to-4-line decoders/demultiplexers
- Schottky clamped for high performance
- Typical propagation delay (3 levels of logic)
  - DM74LS138 21 ns
  - DM74LS139 21 ns
- Typical power dissipation
  - DM74LS138 32 mW
  - DM74LS139 34 mW

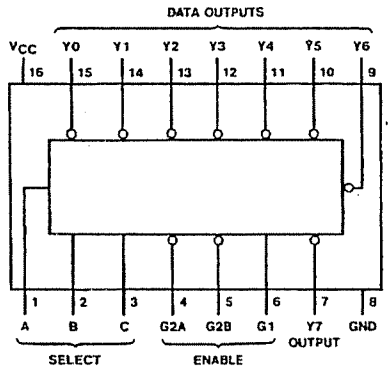
Ordering Code:

Order Number	Package Number	Package Description
DM74LS138M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS138SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS138N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
DM74LS139M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150 Narrow
DM74LS139SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
DM74LS139N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

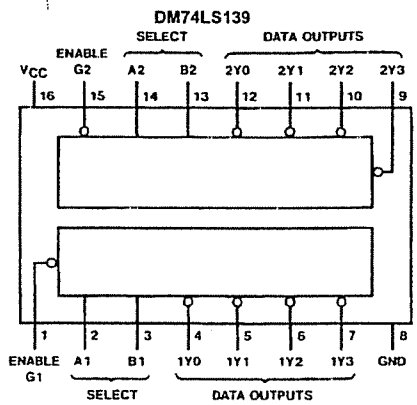
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagrams

DM74LS138



DM74LS139



Function Tables

DM74LS138

Inputs					Outputs							
Enable		Select										
G1	G2 (Note 1)	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	H	L	H	H	H	H
H	L	H	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	H	L	H	H	H	H	H	H	L	H
H	L	H	H	H	H	H	H	H	H	H	H	L

DM74LS139

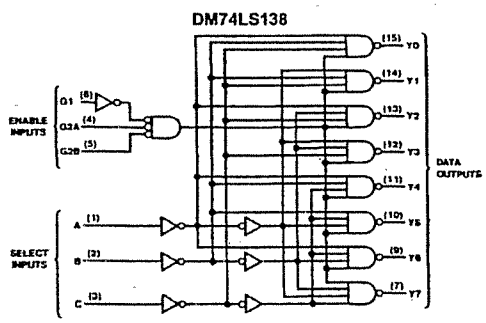
Inputs			Outputs			
Enable	Select					
G	B	A	Y0	Y1	Y2	Y3
H	X	X	H	H	H	H
L	L	L	L	H	H	H
L	L	H	H	L	H	H
L	H	L	H	H	L	H
L	H	H	H	H	H	L

H = HIGH Level
L = LOW Level
X = Don't Care

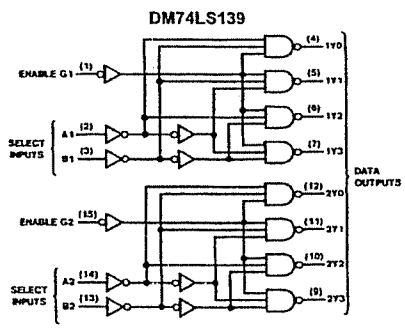
Note 1: G2 = G2A + G2B

Logic Diagrams

DM74LS138



DM74LS139



FAIRCHILD SEMICONDUCTOR™

August 1986
Revised March 2002

DM74LS393
Dual 4-Bit Binary Counter

General Description

Each of these monolithic circuits contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters in a single package. The DM74LS393 comprises two independent four-bit binary counters each having a clear and a clock input. N-bit binary counters can be implemented with each package providing the capability of divide-by-256. The DM74LS393 has parallel outputs from each counter stage so that any submultiple of the input count frequency is available for system-timing signals.

Features

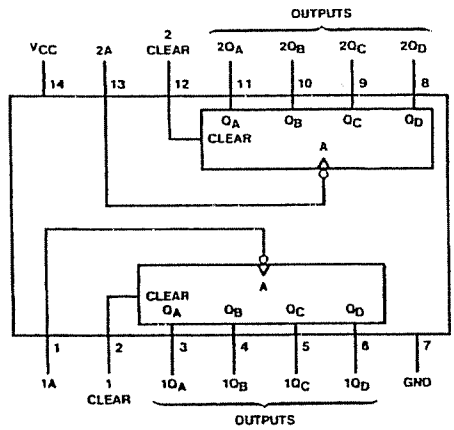
- Dual version of the popular DM74LS93
- DM74LS393 dual 4-bit binary counter with individual clocks
- Direct clear for each 4-bit counter
- Dual 4-bit versions can significantly improve system densities by reducing counter package count by 50%
- Typical maximum count frequency 35 MHz
- Buffered outputs reduce possibility of collector commutation

Ordering Code:

Order Number	Package Number	Package Description
DM74LS393M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
DM74LS393N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



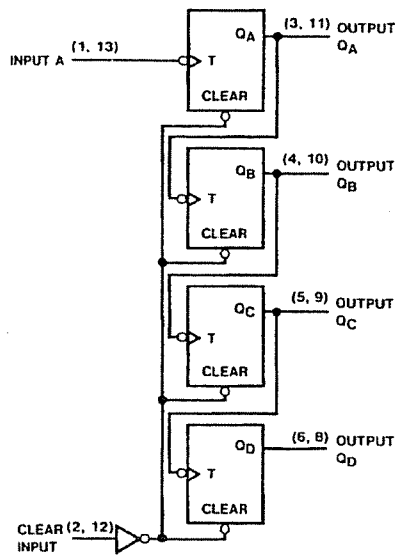
Function Table

Counter Sequence (Each Counter)

Count	Outputs			
	Q_D	Q_C	Q_B	Q_A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

H = HIGH Logic Level
L = LOW Logic Level

Logic Diagram

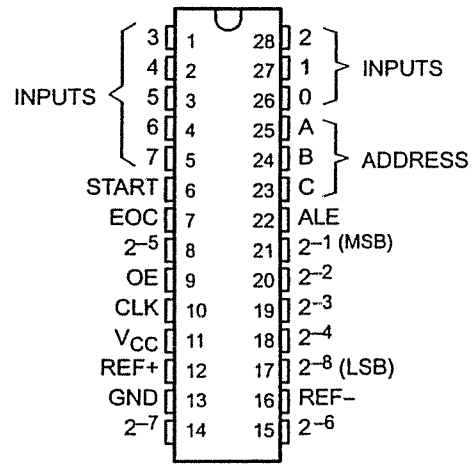


ADC0808, ADC0809
CMOS ANALOG-TO-DIGITAL CONVERTERS WITH 8-CHANNEL MULTIPLEXERS

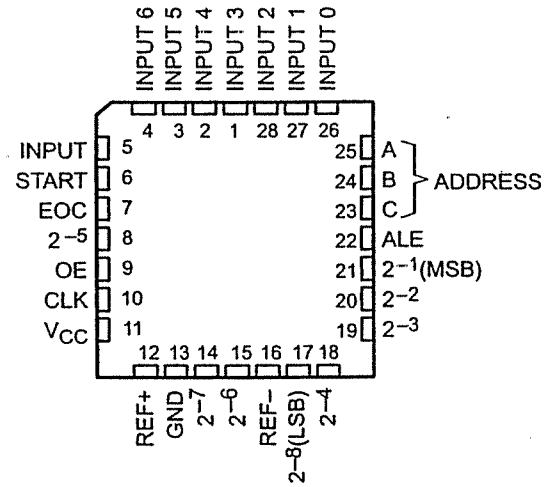
SLAS036 – JUNE 1981 – REVISED MAY 1988

- **Total Unadjusted Error . . . ±0.75 LSB Max for ADC0808 and ±1.25 LSB Max for ADC0809**
- **Resolution of 8 Bits**
- **100-μs Conversion Time**
- **Ratiometric Conversion**
- **Monotonicity Over the Entire A/D Conversion Range**
- **No Missing Codes**
- **Easy interface with Microprocessors**
- **Latched 3-State Outputs**
- **Latched Address inputs**
- **Single 5-V Supply**
- **Low Power Consumption**
- **Designed to Be Interchangeable With National Semiconductor ADC0808, ADC0809**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



description

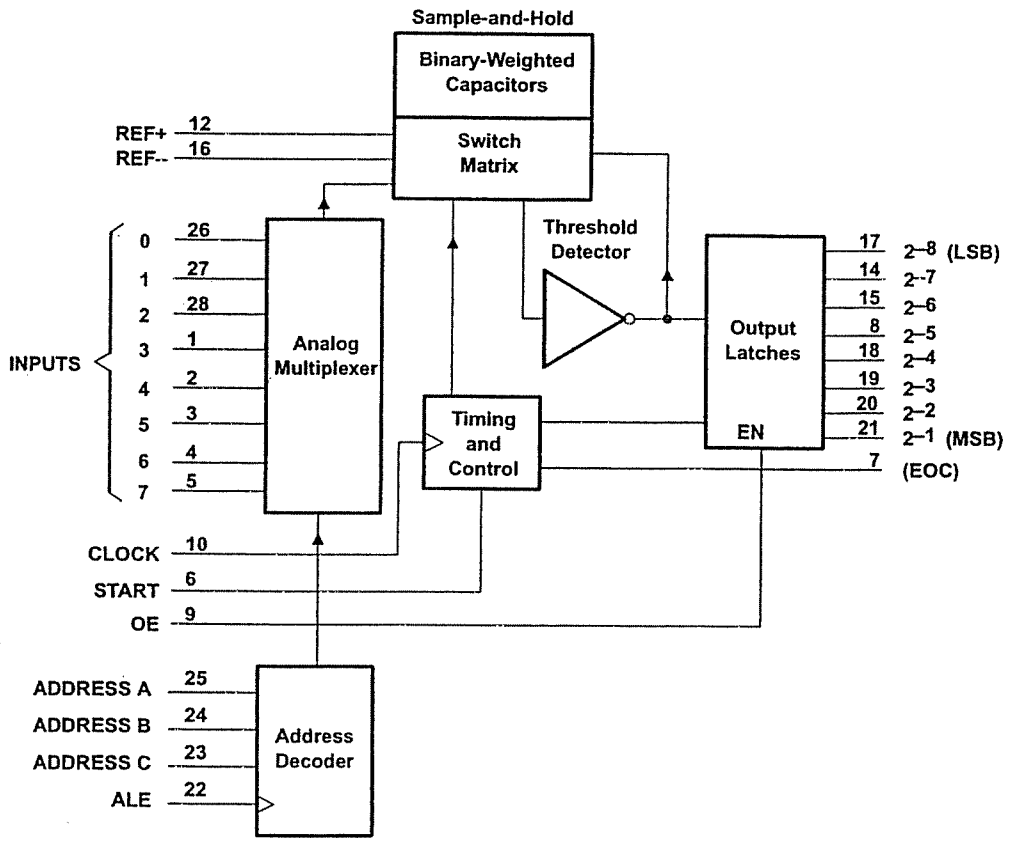
The ADC0808 and ADC0809 are monolithic CMOS devices with an 8-channel multiplexer, an 8-bit analog-to-digital (A/D) converter, and microprocessor-compatible control logic. The 8-channel multiplexer can be controlled by a microprocessor through a 3-bit address decoder with address load to select any one of eight single-ended analog switches connected directly to the comparator. The 8-bit A/D converter uses the successive-approximation conversion technique featuring a high-impedance threshold detector, a switched-capacitor array, a sample-and-hold, and a successive-approximation register (SAR). Detailed information on interfacing to most popular microprocessors is readily available from the factory.

The comparison and converting methods used eliminate the possibility of missing codes, nonmonotonicity, and the need for zero or full-scale adjustment. Also featured are latched 3-state outputs from the SAR and latched inputs to the multiplexer address decoder. The single 5-V supply and low power requirements make the ADC0808 and ADC0809 especially useful for a wide variety of applications. Ratiometric conversion is made possible by access to the reference voltage input terminals.

The ADC0808 and ADC0809 are characterized for operation from −40°C to 85°C.

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265
POST OFFICE BOX 1443 • HOUSTON, TEXAS 77251–1443

functional block diagram (positive logic)

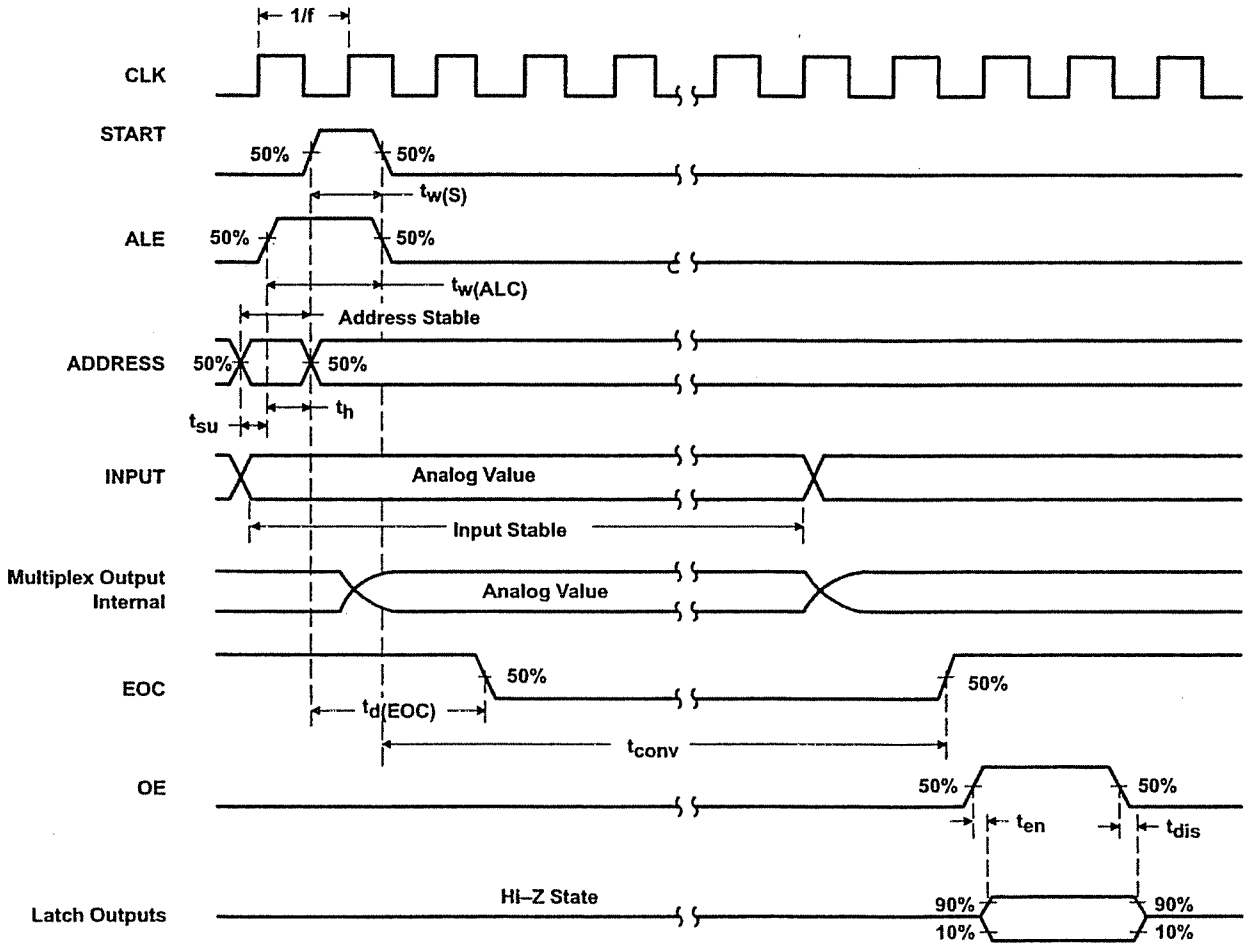


FUNCTION TABLE

INPUTS				SELECTED ANALOG CHANNEL
ADDRESS			ALE	
C	B	A		
L	L	L	↑	0
L	L	H	↑	1
L	H	L	↑	2
L	H	H	↑	3
H	L	L	↑	4
H	L	H	↑	5
H	H	L	↑	6
H	H	H	↑	7

H = high level, L = low level
↑ = low-to-high transition

operating sequence



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) ..... 6.5 V
Input voltage range: Control inputs ..... −0.3 V to 15 V
All other inputs ..... −0.3 V to V_{CC} + 0.3 V
Operating free-air temperature range ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Case temperature for 10 seconds: FN package ..... 260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: N package ..... 260°C

NOTE 1: All voltage values are with respect to network ground terminal.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	4.5	5	6	V
Positive reference voltage, V_{ref+} (see Note 2)		V_{CC}	V_{CC}+0.1	V
Negative reference voltage, V_{ref-}		0	−0.1	V
Differential reference voltage, $V_{ref+} - V_{ref-}$		5		V
High-level input voltage, V_{IH}	V_{CC}−1.5			V
Low-level input voltage, V_{IL}			1.5	V
Operating free-air temperature, T_A	−40		85	°C

NOTE 2: Care must be taken that this rating is observed even during power-up.

electrical characteristics over recommended operating free-air temperature range. V_{CC} = 4.75 V to 5.25 V (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage		I_O = −360 µA	V_{CC}−0.4			V
V_{OL}	Low-level output voltage	Data outputs	I_O = 1.6 mA			0.45	V
		End of conversion	I_O = 1.2 mA			0.45	
I_{OZ}	Off-state (high-impedance-state) output current		$V_O = V_{CC}$			3	µA
			V_O = 0			−3	
I_I	Control input current at maximum input voltage		V_I = 15 V			1	µA
I_{IL}	Low-level control input current		V_I = 0			−1	µA
I_{CC}	Supply current		f_{clock} = 640 kHz		0.3	3	mA
C_i	Input capacitance, control inputs		T_A = 25°C		10	15	pF
C_O	Output capacitance, data outputs		T_A = 25°C		10	15	pF
	Resistance from REF+ to REF−				1000		kΩ

† Typical values are at V_{CC} = 5 V and T_A = 25°C.

analog multiplexer

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I_{on}	Channel on-state current (see Note 3)	$V_I = V_{CC}$,	f_{clock} = 640 kHz			2	µA
		V_I = 0.1 V,	f_{clock} = 640 kHz			−2	
I_{off}	Channel off-state current	V_{CC} = 5 V, T_A = 25°C	V_I = 5 V		10	200	nA
			V_I = 0		−10	−200	
		V_{CC} = 5 V	V_I = 5 V			1	µA
			V_I = 0			−1	

† Typical values are at V_{CC} = 5 V and T_A = 25°C.
NOTE 3: Channel on-state current is primarily due to the bias current into or out of the threshold detector, and it varies directly with clock frequency.

timing requirements, $V_{CC} = V_{ref+} = 5$ V, $V_{ref-} = 0$ V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{clock}	Clock frequency		10	640	1280	kHz
t_{conv}	Conversion time	See Note 4	90	100	116	µs
$t_{w(s)}$	Pulse duration, START		200			ns
$t_{w(ALE)}$	Pulse duration ALE		200			ns
t_{su}	Setup time, ADDRESS		50			ns
t_h	Hold time, ADDRESS		50			ns
t_d	Delay time, EOC	See Notes 4 and 5	0		14.5	µs

operating characteristics, $T_A = 25°C$, $V_{CC} = V_{ref+} = 5$ V, $V_{ref-} = 0$ V, $f_{clock} = 640$ kHz (unless otherwise noted)

PARAMETER		TEST CONDITIONS	ADC0808			ADC0809			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
k_{SVS}	Supply voltage sensitivity	$V_{CC} = V_{ref+}$ = 4.75 V to 5.25 V, T_A = −40°C to 85°C, See Note 6		±0.05			±0.05		%/V
	Linearity error (see Note 7)			±0.25			±0.5		LSB
	Zero error (see Note 8)			±0.25			±0.25		LSB
	Total unadjusted error (see Note 9)	T_A = 25°C		±0.25	±0.5		±0.5		LSB
		T_A = −40°C to 85°C			±0.75			±1.25	
		T_A = 0°C to 70°C						±1	
t_{en}	Output enable time	C_L = 50 pF, R_L = 10 kΩ		80	250		80	250	ns
t_{dis}	Output disable time	C_L = 10 pF, R_L = 10 kΩ		105	250		105	250	ns

† Typical values for all except supply voltage sensitivity are at V_{CC} = 5 V, and all are at T_A = 25°C.
NOTES: 4. Refer to the operating sequence diagram.
5. For clock frequencies other than 640 kHz, $t_{d(EOC)}$ maximum is 8 clock periods plus 2 µs.
6. Supply voltage sensitivity relates to the ability of an analog-to-digital converter to maintain accuracy as the supply voltage varies. The supply and V_{ref+} are varied together and the change in accuracy is measured with respect to full-scale.
7. Linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic.
8. Zero error is the difference between 00000000 and the converted output for zero input voltage; full-scale error is the difference between 11111111 and the converted output for full-scale input voltage.
9. Total unadjusted error is the maximum sum of linearity error, zero error, and full-scale error.

International
IOR Rectifier

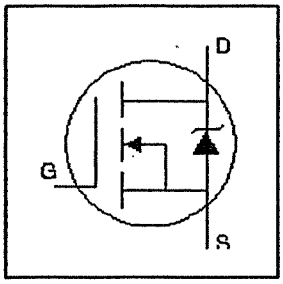
PD - 9.1351

PRELIMINARY

IRF530N

HEXFET® Power MOSFET

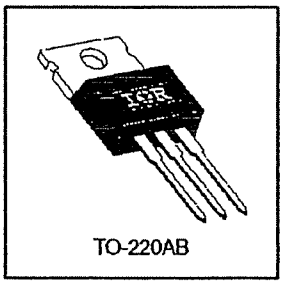
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated



V_{DSS} = 100V

$R_{DS(on)}$ = 0.11Ω

I_D = 15A



TO-220AB

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	15	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	11	
I_{DM}	Pulsed Drain Current ①	60	
P_D @T_C = 25°C	Power Dissipation	63	W
	Linear Derating Factor	0.42	W/°C
V_{GS}	Gate-to-Source Voltage	±20	V
E_{AS}	Single Pulse Avalanche Energy ②	150	mJ
I_{AR}	Avalanche Current①	9.0	A
E_{AR}	Repetitive Avalanche Energy①	6.3	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.2	V/ns
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	——	2.4	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	——	0.50	——	
$R_{\theta JA}$	Junction-to-Ambient	——	——	62	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	100	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.12	—	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	0.11	Ω	V_{GS} = 10V, I_D = 9.0A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	6.4	—	—	S	V_{DS} = 50V, I_D = 9.0A
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	µA	V_{DS} = 100V, V_{GS} = 0V
		—	—	250		V_{DS} = 80V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	—	—	-100		V_{GS} = -20V
Q_g	Total Gate Charge	—	—	44	nC	I_D = 9.0A
Q_{gs}	Gate-to-Source Charge	—	—	6.2		V_{DS} = 80V
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	21		V_{GS} = 10V, See Fig. 6 and 13 ④
$t_{d(on)}$	Turn-On Delay Time	—	6.4	—	ns	V_{DD} = 50V
t_r	Rise Time	—	27	—		I_D = 9.0A
$t_{d(off)}$	Turn-Off Delay Time	—	37	—		R_G = 12Ω
t_f	Fall Time	—	25	—		R_D = 5.5Ω, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	640	—	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	—	160	—		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	—	88	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	15	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	60		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J = 25°C, I_S = 9.0A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	130	190	ns	T_J = 25°C, I_F = 9.0A
Q_{rr}	Reverse Recovery Charge	—	650	970	nC	di/dt = 100A/µs ④

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 3.1mH R_G = 25Ω, I_{AS} = 9.0A. (See Figure 12)

③ I_{SD} ≤ 9.0A, di/dt ≤ 520A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

FAIRCHILD
SEMICONDUCTOR™

September 1983
Revised February 1999

MM74HC14
Hex Inverting Schmitt Trigger

General Description

The MM74HC14 utilizes advanced silicon-gate CMOS technology to achieve the low power dissipation and high noise immunity of standard CMOS, as well as the capability to drive 10 LS-TTL loads.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Typical propagation delay: 13 ns
- Wide power supply range: 2–6V
- Low quiescent current: 20 µA maximum (74HC Series)
- Low input current: 1 µA maximum
- Fanout of 10 LS-TTL loads
- Typical hysteresis voltage: 0.9V at V_{CC} = 4.5V

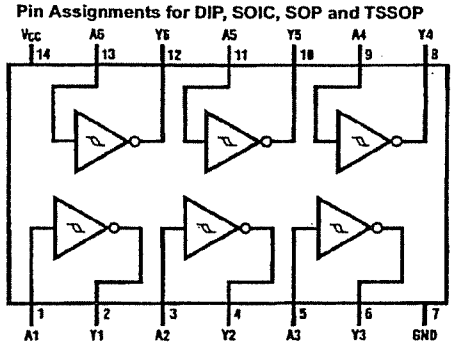
Ordering Code:

Order Number	Package Number	Package Description
MM74HC14M	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-120, 0.150" Narrow
MM74HC14SJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC14MTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC14N	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

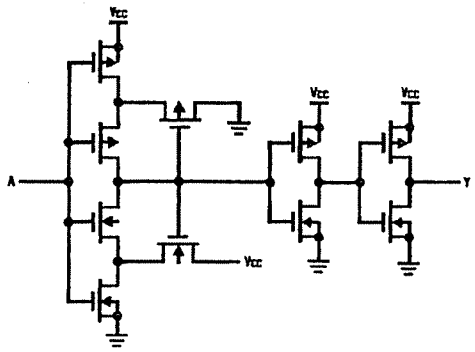
Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



Top View

Logic Diagram



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±25 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±50 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{T+}	Positive Going Threshold Voltage	Minimum	2.0V	1.2	1.0	1.0	1.0	V
			4.5V	2.7	2.0	2.0	2.0	V
			6.0V	3.2	3.0	3.0	3.0	V
		Maximum	2.0V	1.2	1.5	1.5	1.5	V
			4.5V	2.7	3.15	3.15	3.15	V
			6.0V	3.2	4.2	4.2	4.2	V
V_{T-}	Negative Going Threshold Voltage	Minimum	2.0V	0.7	0.3	0.3	0.3	V
			4.5V	1.8	0.9	0.9	0.9	V
			6.0V	2.2	1.2	1.2	1.2	V
		Maximum	2.0V	0.7	1.0	1.0	1.0	V
			4.5V	1.8	2.2	2.2	2.2	V
			6.0V	2.2	3.0	3.0	3.0	V
V_H	Hysteresis Voltage	Minimum	2.0V	0.5	0.2	0.2	0.2	V
			4.5V	0.9	0.4	0.4	0.4	V
			6.0V	1.0	0.5	0.5	0.5	V
		Maximum	2.0V	0.5	1.0	1.0	1.0	V
			4.5V	0.9	1.4	1.4	1.4	V
			6.0V	1.0	1.5	1.5	1.5	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IL} $\lvert I_{OUT}\rvert$ = 20 µA	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
		V_{IN} = V_{IL}						
		$\lvert I_{OUT}\rvert$ = 4.0 mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert$ = 5.2 mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} $\lvert I_{OUT}\rvert$ = 20 µA	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
		V_{IN} = V_{IH}						
		$\lvert I_{OUT}\rvert$ = 4.0 mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert$ = 5.2 mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA	6.0V		2.0	20	40	µA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.